DETAILED ACTION

In view of the appeal brief filed on 7/30/2008, PROSECUTION IS HEREBY REOPENED. A new rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 4-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claimed limitation of "a tunnel junction layer", as recited in dependent claim 5, is unclear as to the structural relationship between the tunnel junction layer and the memory array.

The claimed limitation of "a tunnel junction layer thickness of about 3-5 nanometers", as recited in dependent claim 5, is unclear as to which claimed element has the thickness of about 3-5 nanometers.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-6, 8-11,16, 26-33, 38-41, 47-49 and 55-59, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (6,881,994) in view of Bhattacharyya (7,012,297), Wolf et al. (4,717,943) and Bass Jr. et al. (4,870,470), **or in the alternative**, over Bass Jr. et al. in view of Lee et al. (6,881,994) and Rinerson et al. (6,834,008).

Lee et al. teach in figure 34 and related text a memory array comprising:

a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points (see e.g. figure 52), and

b) a memory cell disposed at each cross-point, each memory cell having exactly two terminals and having a storage element and a control element coupled in series between a row conductor and a column conductor, each control element including a tunnel junction and a silicon oxide insulator.

Lee et al. do not teach a control element including a tunnel junction and a silicon-rich oxide insulator, wherein the silicon rich insulator injects current into the tunnel junction when the memory cell is selected.

Bhattacharyya teach in figure 11 and related text a control element including a tunnel junction and a silicon-rich oxide insulator 1154, wherein the silicon rich insulator injects current into the tunnel junction when the memory cell is selected.

Wolf et al. teach in figure 2 and related text a control element including a tunnel junction 16 and a silicon-rich oxide insulator 20, wherein the silicon rich insulator injects current into the tunnel junction when the memory cell is selected.

Bass Jr. et al. teach in figure 6 and related text a control element including a tunnel junction and a silicon-rich oxide insulator 35, wherein the silicon rich insulator injects current into the tunnel junction when the memory cell is selected.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a control element including a silicon-rich oxide insulator, wherein the silicon rich insulator injects current into the tunnel junction when the memory cell is selected in Lee et al.'s device in order to improve the device characteristics by enhancing the electric field of the structure.

The combination is motivated by the teachings of Bhattacharyya who points out the advantages of using a silicon-rich oxide insulator.

Note further that it is well known in the art to use silicon rich dielectric injectors in the control element of a memory device.

In the alternative:

Bass Jr. et al. teach in figure 6 and related text a memory array (see e.g. abstract) comprising:

a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points (inherent in an array structure), and

b) a memory cell disposed therein, each memory cell having two terminals and having a storage element and a control element coupled in series between a row conductor and a column conductor, each control element including a tunnel junction and a silicon-rich oxide insulator 30 or 35, wherein the silicon rich insulator injects current into the tunnel junction when the memory cell is selected.

Bass Jr. et al. do not teach using the memory structure as a memory cell disposed at each cross-point, wherein each memory cell having exactly two terminals.

Lee et al. teach in figure 34 and related text a memory cell disposed at each cross-point, wherein each memory cell having exactly two terminals.

Rinerson et al. teach in figures 1-3 and related text a memory cell 115, 215, 315 disposed at each cross-point, wherein each memory cell having exactly two terminals.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the memory cell at each cross-point, wherein each memory cell having exactly two terminals in Lee et al.'s device in order to improve the device characteristics by using cross point architecture.
The combination is motivated by the teachings of Rinerson et al. who point out the advantages of using cross point architecture.

Regarding claims 5-6 and 8-10, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a control element of each memory cell comprises a tunnel junction layer thickness of about 3-5 nanometers, and the storage element of each memory cell comprises an anti-fuse, a fuse, a tunnel junction, a state-change layer and a chalcogenide, in prior art's device in order to use known memory control and storage elements, of which official notice is taken.

Regarding claim 11, prior art's device includes a row conductors are arranged in mutually orthogonal relationship with the column conductors.

Regarding claim 16, prior art's device includes a memory cell disposed at each cross-point, each memory cell comprising means for storing data and means for controlling the means for storing data, the means for storing data and means for controlling being coupled in series between a row conductor and a column conductor, and each means for controlling including a silicon-rich insulator.

Regarding claim 26, prior art's device includes a tunnel-junction layer SiN over the silicon rich insulator and a second conductive layer over the tunnel-junction layer. Prior art does not state that the memory cell is formed by a method of

b) depositing and patterning a first conductive layer over the substrate, and

c) forming and patterning a second conductive layer,

However, these process limitations would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claim 38, prior art's device includes a first interlayer dielectric over the storage layer and having an opening through the first interlayer dielectric and extending to the storage layer, and having a conductive material therein as a middle electrode, this conductive layer is contiguous with the storage layer.

Prior art does not state that the memory cell is formed by a method of

b) depositing and patterning a first conductive layer over the substrate, and

c) forming and patterning a second conductive layer,

d) forming and patterning first and second interlayer dielectrics over the storage layer,

e) forming an opening through the first interlayer dielectric and extending to the storage layer,

g) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode.

However, these process limitations would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Regarding claims 30, 47 and 55, prior art's device includes a second interlayer dielectric is formed over the storage layer, forming vias as required though the second interlayer dielectric to selectively interconnect memory cells of the memory arrays.

Prior art does not state that the memory cell is formed by a method of

b) depositing and patterning a first conductive layer over the substrate, and

c) forming and patterning a second conductive layer,

d) forming and patterning first and second interlayer dielectrics over the storage layer,

e) forming an opening through the first interlayer dielectric and extending to the storage layer,

g) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode.

k) forming vias as required though the second interlayer dielectric, and repeating steps b) through k) until a desired number of memory array layers have been formed. However, these process limitations would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. Regarding claims 27-29, 31-33, 39-41, 48-49 and 56-57, prior art's device includes a memory array comprising a multiplicity of the memory cells, a substrate carrying electronics and an IC comprising a multilayer memory, wherein a multiplicity of the memory arrays are arranged in memory layers.

Regarding claims 58-59, prior art's device includes two terminals of the two terminal memory cell disposed at each cross-point comprise the row conductor and column conductor respectively.

Response to Arguments

Applicant's arguments with respect to claims 1, 3-6, 8-11,16, 26-33, 38-41, 47-49 and 55-59 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-4670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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10/18/2008

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